METHODS OF FABRICATING A SEMICONDUCTOR DEVICE HAVING MULTI-GATE INSULATION LAYERS AND SEMICONDUCTOR DEVICES FABRICATED THEREBY

ABSTRACT OF THE DISCLOSURE

Methods of fabricating a semiconductor device having multi-gate insulation layers and semiconductor devices fabricated thereby are provided. The method includes forming a pad insulation layer and an initial high voltage gate insulation layer on a first region and a second region of a semiconductor substrate respectively. The initial high voltage gate insulation layer is formed to be thicker than the pad insulation layer. A first isolation layer that penetrates the pad insulation layer and is buried in the semiconductor substrate is formed to define a first active region in the first region, and a second isolation layer that penetrates the initial high voltage gate insulation layer and is buried in the semiconductor substrate is formed to define a second active region in the second region. The pad insulation layer is then removed to expose the first active region. A low voltage gate insulation layer is formed on the exposed first active region. Accordingly, it can minimize a depth of recessed regions (dent regions) to be formed at edge regions of the first isolation layer during removal of the pad insulation layer, and it can prevent dent regions from being formed at edge regions of the second isolation layer.